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# A NOVEL ENCAPSULATION METHOD FOR SBGA

## BACKGROUND OF THE INVENTION

### (1) FIELD OF THE INVENTION

The present invention relates to methods of packaging integrated circuit devices, and more particularly, to methods of packaging integrated circuit devices without die corner delamination.

### (2) DESCRIPTION OF THE PRIOR ART

In the assembly of integrated circuit devices, super ball grid array (SBGA) techniques have become widely used to electrically attach component packages and to mount them on interconnection substrates such as interposer or printed circuit boards. For example, Fig. 1A shows in top view and Fig. 1B shows a cross-sectional view of a SBGA substrate 10. An integrated circuit chip 12 has been mounted on the SBGA substrate. Now, the chip 12 is to be encapsulated with a liquid resin, for example, to protect the chip. This is especially important for low dielectric constant material wafers since they are very expensive. For example, a low-k wafer has a dielectric material more brittle than fluorinated silicate glass (FSG).

A high viscosity material is applied as a dam 14. Then an encapsulation material is dispensed within the area surrounded by the dam, as shown by 16 in Figs. 2A and 2B. The encapsulation material has a lower viscosity than the dam material. However, thermal cycling testing shows that the liquid encapsulation material 16 suffers delamination at the die corner due to shrinking of the encapsulation layer. High global stress is found at the die corner. This is caused by the mismatch between the coefficient of thermal expansion of the die and the encapsulation material.

Fig. 3 shows an enlarged view of the die 12 showing shrinking 22 of the encapsulation material 16 during curing. Layer 18 represents the active metal circuit layers. The encapsulation material peels up from the surface of the substrate as shown in 20. It is desired to find a way to prevent delamination at the die corner in order to enhance the reliability and yield of SBGA assembly.

U.S. Patents 6,127,724 to DiStefano and 6,020,218 to Shim et al show conventional encapsulation methods. U.S. Patent 6,537,482 to Farnsworth teaches encapsulating the die with a resin. The references do not teach ways of preventing delamination at the die corner.

## SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the invention to provide an effective and very manufacturable process of encapsulating an integrated circuit chip.

Another object of the present invention is to provide a method for encapsulating an integrated circuit chip for assembly into SBGA packaging.

Yet another object of the present invention is to provide a method for encapsulating an integrated circuit chip that prevents die corner delamination.

A further object is to provide a method for encapsulating an integrated circuit chip by applying a low coefficient of thermal expansion material to cover the die corner prior to applying the encapsulation material.

In accordance with the objects of this invention, a method for encapsulating an integrated circuit chip is achieved. An integrated circuit chip is attached to a substrate. A dam is formed surrounding the integrated circuit chip. All corners of the integrated circuit chip are covered with a stress buffering material. The integrated

circuit chip and all of the substrate within the dam are coated with an encapsulation material wherein the encapsulation material covers the stress buffering material and wherein the stress buffering material prevents delamination of the encapsulation material at the corners of the integrated circuit chip.

## BRIEF DESCRIPTION OF THE DRAWINGS

In the following drawings forming a material part of this description, there is shown:

Figs. 1A and 2A are top views of an integrated circuit chip assembly of the prior art.

Fig. 1B is a schematic cross-sectional representation of Fig. 1A of the prior art.

Fig. 2B is a schematic cross-sectional representation of Fig. 2A of the prior art.

Fig. 3 is an enlarged cross-sectional representation showing delamination of the prior art.

Figs. 4A and 5A are top views of an integrated

circuit chip assembly of the present invention.

Fig. 4B is a schematic cross-sectional representation of Fig. 4A of the present invention.

Fig. 5B is a schematic cross-sectional representation of Fig. 5A of the present invention.

Fig. 6 is an oblique view of the die corner in the present invention.

Fig. 7 is an enlarged cross-sectional representation of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention provides a method for encapsulating an integrated circuit chip where corner delamination is prevented. An SBGA substrate is used as an example to explain the process of the invention. It will be understood by those skilled in the art that the process of the invention will be useful with other similar substrates.

Referring now more particularly to Figs. 4A and 4B, there is shown an SBGA substrate 10. An integrated circuit chip 12 has been mounted on the SBGA substrate. A high viscosity material is applied as a dam 14. This material may be an epoxy. Now, in a key step of the present invention, a high viscosity, low coefficient of thermal expansion (CTE) material 30 is coated on the die corners of the chip 12. This material may also be epoxy or resin. There is a low CTE mismatch between the die and the material 30 because both the die and the material 30 have a similar CTE. Also, there is a small contact area between the die and the material 30. The pre-coating material 30 decreases the global stress on the die corners to a small local stress.

Now, an encapsulation material is dispensed within the area surrounded by the dam, as shown by 32 in Figs. 5A and 5B. This material may be an epoxy or a resin. The material 30 on the die corners acts as a stress buffer during thermal processing to prevent delamination of the encapsulation material at the die corners.

FIg. 6 shows an oblique view of the die corner. Material 30 covers the corner of the die. Fig. 7 is an enlarged cross-sectional view of the chip 12, showing the active metal circuit layer 33. The stress buffer material

layer 30 is shown covering the corner of the die. Encapsulation material 32 covers the entire die.

The process of the present invention prevents delamination of the encapsulation material at the die corners by covering the die corners with a stress buffer material prior to encapsulation.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: